EXHIBIT 5

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
90/014,831	08/23/2021	7499042	034960.0038-US01	7318

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JAMESMILKEY
12424 WILSHIRE BLVD,
12TH FLOOR
LOS ANGELES, CA 90025

EXAMINER	
GE, YUZHEN	

ART UNIT	PAPER NUMBER
3992	

MAIL DATE	DELIVERY MODE
02/02/2022	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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EX PARTE REEXAMINATION COMMUNICATION TRANSMITTAL FORM

REEXAMINATION CONTROL NO. *90/014,831* .

PATENT UNDER REEXAMINATION *7499042* .

ART UNIT *3992* .

Enclosed is a copy of the latest communication from the United States Patent and Trademark Office in the above identified *ex parte* reexamination proceeding (37 CFR 1.550(f)).

Where this copy is supplied after the reply by requester, 37 CFR 1.535, or the time for filing a reply has passed, no submission on behalf of the *ex parte* reexamination requester will be acknowledged or considered (37 CFR 1.550(g)).

Office Action in Ex Parte Reexamination	Control No. 90/014,831	Patent Under Reexamination 7499042	
	Examiner YUZHEN GE	Art Unit 3992	AIA (FITF) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

a. ☐ Responsive to the communication(s) filed on _____.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

b. ☐ This action is made FINAL.

c. ☑ A statement under 37 CFR 1.530 has not been received from the patent owner.

A shortened statutory period for response to this action is set to expire 2 month(s) from the mailing date of this letter. Failure to respond within the period for response will result in termination of the proceeding and issuance of an *ex parte* reexamination certificate in accordance with this action. 37 CFR 1.550(d). **EXTENSIONS OF TIME ARE GOVERNED BY 37 CFR 1.550(c).** If the period for response specified above is less than thirty (30) days, a response within the statutory minimum of thirty (30) days will be considered timely.

Part I THE FOLLOWING ATTACHMENT(S) ARE PART OF THIS ACTION:

1. ☐ Notice of References Cited by Examiner, PTO-892.
2. ☐ Information Disclosure Statement, PTO/SB/08.
3. ☐ Interview Summary, PTO-474.
4. ☐ _____.

Part II SUMMARY OF ACTION

1a. ☑ Claims 1-6 and 10-11 are subject to reexamination.
1b. ☐ Claims _____ are not subject to reexamination.
2. ☐ Claims _____ have been canceled in the present reexamination proceeding.
3. ☐ Claims _____ are patentable and/or confirmed.
4. ☑ Claims 1-6 and 10-11 are rejected.
5. ☐ Claims _____ are objected to.
6. ☐ The drawings, filed on _____ are acceptable.
7. ☐ The proposed drawing correction, filed on _____ has been (7a) ☐ approved (7b) ☐ disapproved.
8. ☑ Acknowledgment is made of the priority claim under 35 U.S.C. 119(a)-(d) or (f).
   a) ☑ All b) ☐ Some* c) ☐ None of the certified copies have
   1 ☐ been received.
   2 ☐ not been received.
   3 ☑ been filed in Application No. 11/035,269.
   4 ☐ been filed in reexamination Control No. _____.
   5 ☐ been received by the International Bureau in PCT application No. _____.
   * See the attached detailed Office action for a list of the certified copies not received.
9. ☐ Since the proceeding appears to be in condition for issuance of an *ex parte* reexamination certificate except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte* Quayle, 1935 C.D. 11, 453 O.G. 213.
10. ☐ Other: _____

cc: Requester (if third party requester)

EX PARTE REEXAMINATION OF U.S. PATENT 7,499,042

I. ACKNOWLEDGEMENT

On August 23, 2021, Third Party Requester ("**Requester**") filed a request ("**Request**") for *ex parte* reexamination of claims 1-6 and 10-11 ("**Requested Claims**") of US Patent 7,499,042 ("**the `042 Patent**") which was issued to Shirasaki et al with title "Device, Data Driving Circuit, And Display Panel Driving Method." The `042 Patent was filed on Jan. 12, 2005 with application number 11/035,269 ("**the 269 Application**") and issued on Mar. 3, 2009 with claims 1-11.

On Sept. 8, 2021, the Office mailed an order ("2021 Order") granting reexamination of claims 1-6 and 10-11 of the `042 Patent.

A Patent Owner's statement has not been received after two months that the reexamination is ordered.

II. PRIORITY CLAIMS

This section is the same as that in the 2021 Order.

Based upon a review of the `042 Patent, the Examiner finds that the `042 Patent or the 269 Application claims does not claim any domestic priority but claims foreign priority to JP 2004-009146, filed on Jan. 16, 2004. To the extent that the claims of the `042 Patent are supported by JP 2004-009146, the priority date is Jan. 16, 2004. A certified copy of foreign priority document is in the file of the 269 Application. However an English translation of the foreign priority document is not in the file of the 269 Application.

Because the effective filing date of the `042 Patent is not on or after March 16, 2013, the AIA First Inventor to File ("AIA-FITF") provisions does not apply and the earlier 'First to Invent' provisions apply.

III. PRIOR OR CONCURRENT PROCEEDINGS

This section is the same as that in the 2021 Order.

Based upon Examiner's review of the `042 Patent itself, the Request, and its prosecution history, the Examiner finds that there are no prior or concurrent *ex parte* or supplemental reexaminations for the `042 Patent. There were no prior *inter parte* reviews either. However there are concurrent litigations which are noted in the file.

IV. REFERENCES

i. The article "*Full Color Polymer OLED Display Driven by a-Si:H TFT Utilizing a New Current-Programmed Method*" ("Shirasaki'), published by the Society for Information Display in the Proceedings of the 10th International Display Workshops ("IDW"), and provided to attendees of the conference, held December 3-5, 2003. Shirasaki qualifies as prior art to the `042 Patent under 35 U.S.C. § 102(b).

ii. PCT Application No. WO 2004/001714 ("Sato"), published on Dec. 31, 2003. Sato qualifies as prior art to the `042 Patent under 35 U.S.C. § 102(b).

iii. U.S. Patent Pub No. 2003/0122745 ("Miyazawa"), published on July 3, 2003, Miyazawa qualifies as prior art to the `042 Patent under 35 U.S.C. § 102(b).

V. CLAIM INTERPRETATION

A. Lexicographic Definitions

After careful review of the original specification and unless expressly noted otherwise by the Examiner, the Examiner cannot locate any lexicographic definitions in the original specification with the required clarity, deliberateness, and precision. Because the Examiner cannot locate any lexicographic definitions in the original specification with the required clarity, deliberateness, and precision the Examiner concludes the Patent Owner is not their own lexicographer. See MPEP § 2111.01 IV.

B. Abbreviations

BRI – Broadest Reasonable Interpretation.

POSITA – A person of ordinary skill in the art.

C. 'Sources' for the 'Broadest Reasonable Interpretation'

For terms not lexicographically defined by Patent Owner, the Examiner hereby adopts the following interpretations under the broadest reasonable interpretation standard. In other words, the Examiner has provided the following interpretations simply as express *notice* of how she is interpreting particular terms under the broadest reasonable interpretation standard. Additionally, these interpretations are only a guide to claim terminology since claim terms must be interpreted in context of the surrounding claim language.[1] In accordance with *In re Morris*, 127 F.3d 1048, 1056, 44 USPQ2d 1023, 1029 (Fed. Cir. 1997), the Examiner points to these other "sources" to

[1] While most interpretations are cited because these terms are found in the claims, the Examiner may have provided additional interpretations to help interpret words, phrases, or concepts found in the interpretations themselves, the `042 Patent, or in the prior art.

support her interpretation of the claims. Finally, the following list is not intended to be exhaustive in any way:

1. Circuit: "circuit (1) (A) The physical medium on which signals are carried across the AUI. The data and control circuits consist of an A circuit and a B circuit forming a balanced transmission system so that the signal carried on the B circuit is the inverse of the signal carried on the A circuit. (B) (data transmission) A network providing one or more closed paths. (C) An arrangement of interconnected components that has at least one input and one output terminal, and whose purpose is to produce at the output terminals a signal that is a function of the signal at the input terminals. Synonyms: physical circuit; network. See also: expansion board; channel; telecommunication circuit. (D) An arrangement of interconnected electronic components that can perform specific functions upon application of proper voltages and signals. See also: logic circuit; integrated circuit." – The Authoritative Dictionary of IEEE Standards Terms, 7th Ed., IEEE, Inc., New York, NY.

2. Display: "display device (1) In computer graphics, an output device on which display images can be represented. For example, cathode ray tube display device, plotter, hard copy unit. See also: graphical display device. (2) An output device that gives a visual representation of data. (3) The hardware used to provide the display to users. An example is a video display unit." – The Authoritative Dictionary of IEEE Standards Terms, 7th Ed., IEEE, Inc., New York, NY.

3. Configuration: "(C) The physical and logical elements of an information processing system, the manner in which they are organized and connected, or both. Note: May refer to a hardware configuration or software configuration." The Authoritative Dictionary of IEEE Standards Terms, 7th Ed., IEEE, Inc., New York, NY, 12/2000.

D. 35 U.S.C. § 112 6th Paragraph

The following is a quotation of pre-AIA § 112 ¶ 6:

> An element in a claim for a combination may be expressed as a means or step for performing a specified function without the recital of structure, material, or acts in support thereof, and such claim shall be construed to cover the corresponding structure, material, or acts described in the specification and equivalents thereof.

A second exception is when a claimed phrase is interpreted in accordance with 35 U.S.C. § 112 6th paragraph ("**§ 112 ¶ 6**"). See MPEP § 2181 *et seq*. To invoke § 112 ¶ 6, a claimed phrase must meet the three prong analysis ("**3 Prong Analysis**") as set forth in MPEP § 2181 (I). The following phrases will be first identified and then analyzed using the MPEP's 3 Prong Analysis to determine if the claimed phrases invoke § 112 ¶ 6. If a phrase invokes § 112 ¶ 6, the corresponding structure will also be determined. The Examiner has reviewed the reexamined claims and determines that the following functional phrases invoke § 112 ¶ 6.

1. Functional Phrase #1

> a plurality of pixel circuits which are connected to said plurality of selection scan lines and said plurality of current lines, and supply a driving current having a current value corresponding to the current value of the designating current which flows through said plurality of current lines;
>
> wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines, and stores a level of a voltage converted in accordance with the current value of the designating current, and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

--"**Functional Phrase #1**" or "**FP #1**" – From claim 1 and claim 10.

i. <u>3 Prong Analysis</u>: Invocation Prong (A)

In accordance with Invocation Prong (A), the MPEP states:

> (A) the claim limitation uses the term "means" or "step" or a term used as a substitute for "means" that is a generic placeholder (also called a nonce term or a non-structural term having no specific structural meaning) for performing the claimed function ....
>
> MPEP § 2181 I. — Invocation Prong (A).

As an initial matter, the Examiner finds that Functional Phrase #1 does not use the term "means." Therefore the issue arising under Invocation Prong (A) then becomes whether or not FP#1, including the claimed "pixel circuit [*and* perform the claimed functions]," is a generic placeholder for "means."

In assessing whether or not FP#1 invokes § 112 ¶ 6, the Examiner must not only consider the introductory phrase "pixel circuit," but the entire FP#1. "In assessing whether the claim limitation is in means-plus-function format, we do not merely consider the introductory phrase (e.g., 'mechanical control assembly') in isolation, but look to the entire passage including functions performed by the introductory phrase. [Emphasis added.]" *MTD Prods. Inc. v. Iancu*, 933 F.3d 1336, 1342 (Fed. Cir. 2019).

Second, the Examiner has reviewed the original specification and drawings as set forth in the 269 Application or the`042 Patent, general and subject matter specific dictionaries, and the prior art now of record to determine if they provide a description sufficient to inform one of ordinary skill in this particular art that FP#1 denotes a particular structure.

Third, the Examiner finds that a "pixel circuit" is structure. However the claimed "pixel circuit" as set forth in FP#1 has a particular configuration to perform the claimed functions. In light of the claimed "pixel circuit," the Examiner concludes that the claimed "pixel circuit" is not a generic pixel circuit or a known in the art pixel circuit but a particular pixel circuit requiring

special programming since the specific claimed functions as set forth in FP#1 cannot be performed by a generic pixel circuit known in the art.

In light of the above, the Examiner concludes that the phrase "pixel circuit" performing the claimed functions is a generic placeholder. Because "pixel circuit" is merely a generic placeholder, the Examiner concludes that Functional Phrase #1 meets invocation Prong (A).

ii. 3 Prong Analysis: Invocation Prong (B)

Based upon a review of the Functional Phrase #1, the Examiner finds that for Functional Phrase #1, the claimed function is

> supply a driving current having a current value corresponding to the current value of the designating current which flows through said plurality of current lines;
> wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines, and stores a level of a voltage converted in accordance with the current value of the designating current, and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

--**Function of FP#1.**

Additionally, the Examiner finds that because nothing in the written description of the `042 Patent contradicts the plain language as set forth in the Function of FP#1, Function of FP#1 will have their ordinary and accustomed meaning. Because Functional Phrase #1 includes the Function of FP#1, the Examiner concludes that, Functional Phrase #1 meets invocation prong (B).

iii. 3 Prong Analysis: Invocation Prong (C)

Based upon a review of Functional Phrase #1, the Examiner finds that Functional Phrase #1 does not contain sufficient structure for performing the entire Function of FP#1. In fact, the

Examiner finds that Functional Phrase #1 recites very little structure (if any) for performing the Function of FP#1.

Because Functional Phrase #1 does not contain sufficient structure for performing the entire claimed function, the Examiner concludes that Functional Phrase #1 meets invocation Prong (C).

Because Functional Phrase #1 meets the three prong analysis as set forth in MPEP § 2181 I, the Examiner concludes that Functional Phrase #1 invokes § 112 ¶ 6.

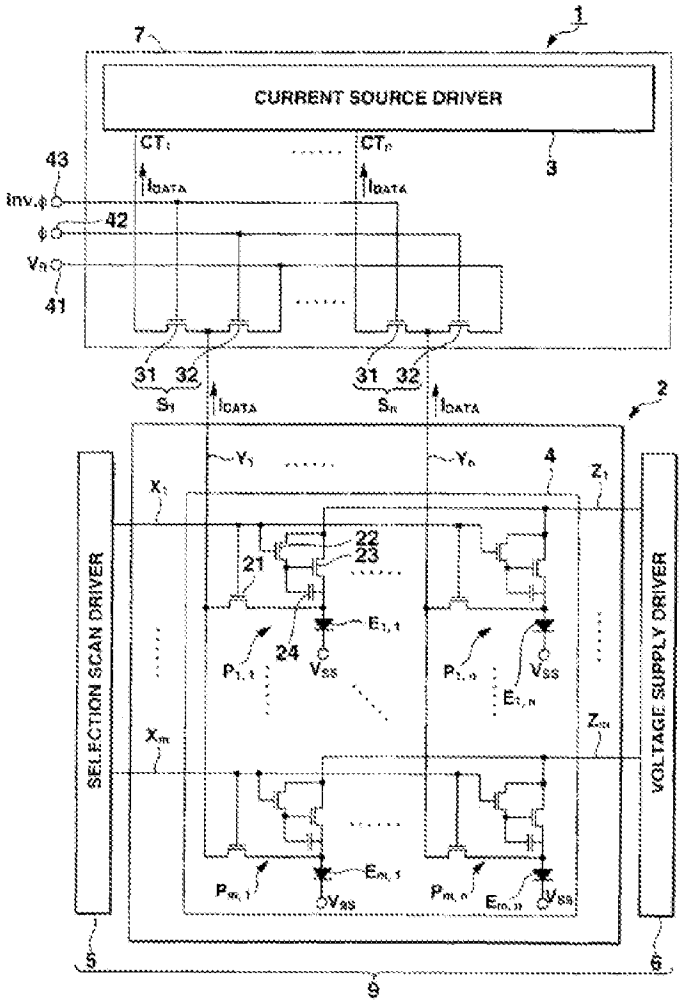

FIG.1

-Fig. 1 of the 042 Patent, showing circuit corresponding to FP#1, i.e., pixel circuits, $P_{i,j}$.

iv. Corresponding Structure or Materials

"The next step in construing a means-plus-function claim limitation is to look to the specification and identify the corresponding structure for that function." *In re Aoyama*, 656 F3d 1293, 99 USPQ2d 1936 (Fed. Cir. 2011) quoting *Golight, Inc. v. Wal-Mart Stores, Inc.*, 355 F.3d 1327, 1333, 1334, [69 USPQ2d 1481, 1486] (Fed. Cir. 2004). "Under this second step, structure disclosed in the specification is `corresponding' structure only if the specification or prosecution history clearly links or associates that structure to the function recited in the claim." *In re Aoyama*, , 99 USPQ2d at 1939 quoting *Med. Instrumentation & Diagnostics Corp. v. Elekta AB*, 344 F.3d 1205, 1210, [68 USPQ2d 1263, 1267] (Fed. Cir. 2003).

Based upon a review of the `042 Patent itself, the Examiner concludes that the corresponding structure for FP#1 is disclosed as the pixel circuit $P_{i,j}$ shown in Figs. 1 and 3 described in 5:25-8:19 of the `042 Patent and the algorithm performed by the pixel circuit is

> supply a driving current having a current value corresponding to the current value of the designating current which flows through said plurality of current lines;
> in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines, and stores a level of a voltage converted in accordance with the current value of the designating current, and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

2. Functional Phrase #2

> a data driving circuit which applies a reset voltage to said plurality of current lines in a first part of the selection period, and supplies a designating current having a current value corresponding to an image signal to said plurality of current lines in a second part of the selection period after applying the reset voltage in the selection period.

--"**Functional Phrase #2**" or "**FP #2**" – From claim 1 and claim 10.

i-iii. 3 Prong Analysis: Invocation Prong (A)-(C)

Similar analysis performed above for FP#1 is also performed for FP#2 and it is Examiner's conclusion that FP#2 invokes § 112 ¶ 6.

iv. Corresponding Structure or Materials

Based upon a review of the `042 Patent itself, the Examiner concludes that the corresponding structure for FP#2 is disclosed as the data driving circuit 7 in Fig. 1 including the input of V_R and ϕ and the algorithm performed by the data driving circuit 7 is "applies a reset voltage to said plurality of current lines in a first part of the selection period, and supplies a designating current having a current value corresponding to an image signal to said plurality of current lines in a second part of the selection period after applying the reset voltage in the selection period."

3. Functional Phrase #3

a current source driver which supplies the designating current having the current value corresponding to the image signal after the reset voltage is applied by the switch within the selection period.

--"**Functional Phrase #3**" or "**FP #3**" – From claim 2.

i-iii. 3 Prong Analysis: Invocation Prong (A)-(C)

Similar analysis performed above for FP#1 is also performed for FP#3 and it is Examiner's conclusion that FP#3 invokes § 112 ¶ 6.

iv. Corresponding Structure or Materials

Based upon a review of the `042 Patent itself, the Examiner concludes that the corresponding structure for FP#3 is disclosed as the current source driver 3 in Fig. 1. The structure of the current source driver is known in the art "to supply the designating current having the current value corresponding to the image signal after the reset voltage is applied by the switch within the selection period" (4:39-43, 11:41-65, *Id*).

4. Functional Phrase #4

a selection scan driver which sequentially selects said plurality of selection scan lines in each selection period

--"**Functional Phrase #4**" or "**FP #4**" – From claim 1.

i-iii. <u>3 Prong Analysis</u>: Invocation Prong (A)-(C)

Similar analysis performed above for FP#1 is also performed for FP#4 and it is Examiner's conclusion that FP#4 invokes § 112 ¶ 6.

iv. Corresponding Structure or Materials

Based upon a review of the `042 Patent itself, the Examiner concludes that the corresponding structure for FP#4 is illustrated as the selection scan driver 5 in Fig. 1-Fig. 12 and described in 9:3-19. That is, the selection scan driver is a "so-called shift register" and "sequentially selects the selection scan lines X_1 to X_m by sequentially outputting selection signals in order from the selection scan line X_1 to the selection scan line X_m (the selection scan line X_m is followed by the selection scan line X_1), thereby sequentially selecting the first and second transistors 21 and 22 in these rows connected to the selection scan lines X_1 to X_m." (9:3-19, *Id*).

v. How To Prevent FP#1-FP#4 From Invoking § 112 ¶ 6

If Patent Owner does not intend to have the claim limitation invoke § 112 ¶ 6, Patent Owner may amend claims 1, 2 and 10 so that they will clearly not invoke § 112 ¶ 6.

Moreover, if Patent Owner believes FP#1-FP#4 have a structural meaning known to a person of ordinary skill in this particular art, Patent Owner should in their next appropriately filed response, expressly state on the record that FP#1-FP#4 have a structural meaning known to a person of ordinary skill in this particular art ***and*** provide appropriate evidence in support thereof (*e.g.* a prior art U.S. patent).

Additionally, in order to show that FP#1-FP#4 do not meet 3 Prong Analysis: Invocation Prong (C), Patent Owner must also state on the record and provide evidence in support thereof that the claimed structure (of FP#1-FP#4 whatever it is) can perform the *entire* Function of FP#1-FP#3.

Patent Owner is reminded that should Patent Owner amend a claimed phrase so that a claimed phrase does not invoke § 112 ¶ 6 or successfully argue that a claimed phrase does not invoke § 112 ¶ 6, elements from the specification (including any algorithms) will ***not*** be read into the claims. "This court [the Federal Circuit] has repeatedly and clearly held that it will not read unstated limitations into claim language." *Northern Telecom Ltd. v. Samsung Elecs. Co.*, 215 F.3d 1281, 1290, 55 USPQ2d 1065, 1072 (Fed. Cir. 2000).

VI. STATUS OF CLAIMS

Based on the Request and the 2021 Order:

Claims 1-6 and 10-11 are being reexamined ("**Reexamined Claims**").

Regarding the Reexamined Claims and as a result of this Office action:

Claims 1-6 and 10-11 are rejected.

VII. CLAIM REJECTIONS - 35 U.S.C. § 103

The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

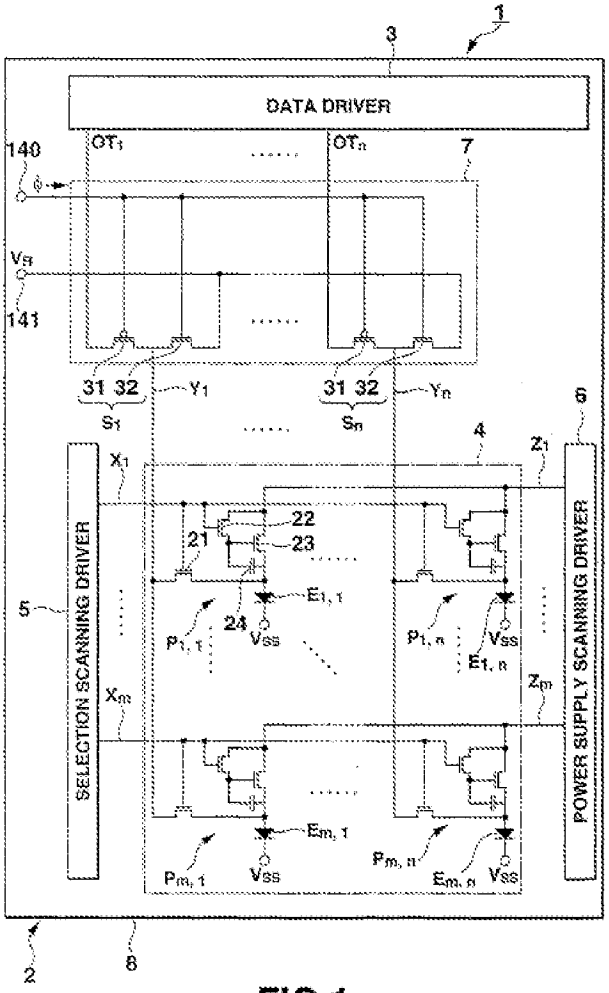

FIG.1

-Fig. 1 of Sato.

A. Claims 1-6 and 10-11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Sato in view of Shirasaki.

Summary of the rejection: The primary reference of Sato discloses the corresponding hardware or circuits required by the claims or the functional phrases of the claims (see Section V Claim Interpretation above) except for the algorithm performed by the data driving circuit in the first part of the selection period and the algorithm performed by the pixel circuits. The secondary reference of Shirasaki discloses the above algorithms not expressly disclosed by Sato.

Regarding claim 1, Sato teaches a display device comprising:

a plurality of selection scan lines (X1-Xm, Fig. 1, pp. 7 and 13);

a plurality of current lines (Y1-Yn, Fig. 1, p. 12);

a selection scan driver which sequentially selects said plurality of selection scan lines in each selection period (5 in Fig. 1. Last paragraph of p. 24, "*The selection scanning driver 5 is formed of a so-called shifter register.*", see also pp. 37 and 39 and the description associated with the selection scanning driver 5 in Fig. 1);

a data driving circuit (Data Driver 3 and the circuit 7) which applies a reset voltage to said plurality of current lines [in a first part of the selection period] (V_R is the reset voltage, pp. 31-32, "*The switch circuits S1 to Sn are connected to a reset voltage input terminal 141, and the reset voltage VR is applied to the switch circuits S1 to Sn via this terminal.*" See also Fig. 8 which shows reset voltage is applied), and supplies a designating current having a current value corresponding to an image signal to said plurality of current lines in a second part of the selection period after applying the reset voltage in the selection period ("*the gradation*

designating current is the sink current flowing to the data driver 3 from the signal lines Y1 to Yn via the current terminals OT_1 *to* O_{Tn}*, and is equal to the current value of the current flowing through the organic EL elements* $E_{1,1}$ *to Em,n in order to emit the light at the luminance gradation in accordance with image data*.", p. 27:5-12, p. 39:9-15, p. 40:16-24, see also Fig. 8); and

a plurality of pixel circuits which are connected to said plurality of selection scan lines and said plurality of current lines (4 in Fig. 1), and supply a driving current having a current value corresponding to the current value of the designating current which flows through said plurality of current lines (Fig. 8, p. 28:15-17, p. 45:4-9, "*in any column of the first to n-th columns, the current value of the driving current flowing through the organic EL elements* $E_{i,1}$ *to* $E_{i,n}$ *in the emission period* T_{EM} *reaches the current value of the gradation designating current flowing through the signal lines* Y_1 *to* Y_n.").

However, Sato does not expressly teach

a data driving circuit which applies a reset voltage to said plurality of current lines in a first part of the selection period;

wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines, and stores a level of a voltage converted in accordance with the current value of the designating current, and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

In the same field of display devices, data driving circuit and display panel driving method, Shirasaki discloses a "*full color polymer OLED display driven by a-Si:H TFT utilizing a*

new current-programmed method" (Shirasaki, title). Shirasaki discloses an OLED display for TV monitor application and "*the panel for this application is required to be driven by an active-matrix (AM) method and to have a larger panel-size*" (INTRODUCTION, *Id*).

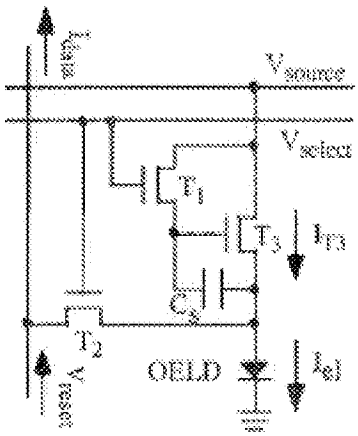

Fig.1 3 Tr pixel driver circuit

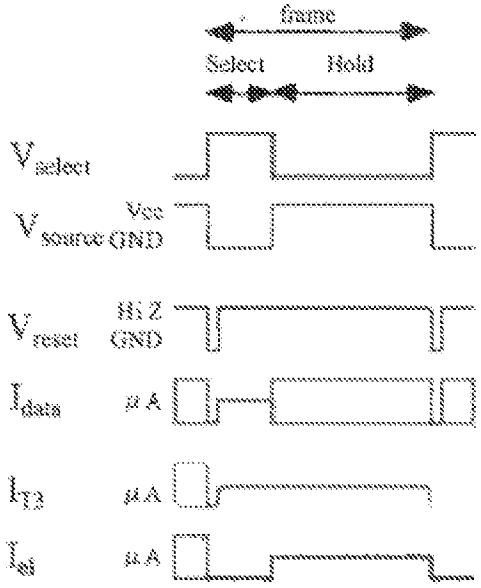

Fig.2 Timing diagram

-Figs. 1 and 2 of Shirasaki.

Shirasaki discloses:

> Figures 1 and 2 show a pixel driver circuit and a timing diagram of the signals, respectively. At the beginning of the select periods, the data line is grounded by V_{reset} to discharge the data line and the OLED anode. Then I_{data} is set to the pixel circuit with a sink mode. To prevent the current flow through the OLED, V_{source} is also grounded and the OLED is biased reversely. Therefore I_{data} corresponds to I_{T3} and C_S stores the voltage to keep the I_{T3}. During the hold period, V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on C_S.

-Pixel Circuit and A set of Timing, p.1 or p. 1665, *Id*.

Table 1 of Shirasaki discloses that its display includes a matrix comprising 160 columns and 128 rows of pixels and its "3-TFT and 3-busline pixel circuits" provided for each of the 160X128 pixels. For example, for each pixel of the display panel, there is one pixel driver circuit shown in Fig. 1. Because Shirasaki discloses a 2.1inch OLED display (Fig. 5) with

plurality of pixels, Shirasaki discloses a plurality of pixel driver circuits. Further, the V_{select} lines are the selection scan lines, and for each row of pixels, there will be one V_{select} line (Fig. 1, *Id*). The I_{data} lines are the current lines and for each column of pixels, there is one I_{data} line (Fig. 1, *Id*) and the I_{data} lines correspond to I_{T3} and Cs stores the voltage to keep the I_{T3}. Shirasaki discloses "a selection scan driver" for V_{select} that provides the signals disclosed in Fig. 2.

Shirasaki discloses that a data driving circuit applies a reset voltage to said plurality of current lines in a first part of the selection period (Fig. 2, Vreset is applied in the first part of the selection period) and each of the "pixel circuits loads the designating current (I_{data}) which flows through said plurality of current line" (Figs. 1 and 2) and each pixel circuit stores a level of a voltage converted in accordance with the current value of the designating current (Cs stores the voltage to keep the I_{T3}, p.1 or p. 1665).

Shirasaki discloses at the end of select period, I_{data} no longer flows to the pixel (Fig. 2, Idata is 0 at the end of the select period). Shirasaki further explains that during the "hold" period (Fig. 2), "V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on Cs" (Fig. 2, p. 1 or p. 1665, *Id*).

Table 1 Specifications

Items	Specification	
Size (Diagonal)	5.2 (2.1)	cm (inch)
Dot format	160(H)×RGB×128(V)	dot
Dot pitch	0.252(H)×0.252(V)	mm
Flame frequency	30	Hz
Color arrangement	RGB-stripe	
Input signal	RGB each 6-bit	
CIE Color Coordinate	R (0.69, 0.31) G (0.40, 0.58) B (0.15, 0.15)	
Contrast Ratio	> 100 : 1	

-Table. 1 of Shirasaki.

As explained above and shown in Figs. 1-2 and above cited paragraph of Shirasaki, Shirasaki discloses or suggests

> a data driving circuit which applies a reset voltage to said plurality of current lines in a first part of the selection period;
> wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines, and stores a level of a voltage converted in accordance with the current value of the designating current, and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current.

TSM-motivation

Shirasaki discloses:

> There are two ways to compensate the TFT threshold voltage variation, current-program [2] and voltage-program [3]. Both of them needed more than four TFTs; and four bus-lines for each pixel. in general, which is too complicated in driving scheme and too busy in pixel aria to achieve the high reliability and large aperture ratio. Simpler circuit design and driving scheme are expected in a-Si TFT driving AM--OLED, In SID'03 three TFT voltage-program pixel circuit was presented using in 20 inch a-Si TFT AM-OLED [4]. This driving technology makes possible to drive large-sized AM-OLED utilizing a-Si TFT.

-Introduction, Shirasaki.

It is desirable to be able to drive a large-size AM-OLED and have a simpler driving scheme to achieve high reliability and large aperture ratio. The disclosure of algorithms by Shirasaki will improve the device of Sato by having a simpler driving scheme and have a high reliability and large aperture ratio. Therefore it would have been obvious to one of ordinary skills in the art, at the time of invention of the `042 Patent to use Shirasaki's method of data driving in the data driving circuits and in the pixel circuits in the display device of Sato so that large-size AM-OLED can be driven with high reliability and large aperture ratio.

KSR-motivation

The combination of Sato with Shirasaki is supported by KSR rationale - (C) Use of known technique to improve similar devices (methods, or products) in the same way because: (1) as discussed above, Sato teaches a base device that is the same as the invention, except for improvements, such as, the features noted as missing above; (2) Sato and Shirasaki are similar devices; and (3) the references show that a POSITA at the time of the invention had the skill set and could apply Shirasaki's method of operating the data driving circuits and pixel circuits to improve the base device of Sato in the same way with predictable results or (B) Simple substitution of one known element for another to obtain predictable results because substituting the algorithm of the data driving circuits and the algorithm of the pixel circuits of Sato by that of Shirasaki will obtain predictable results.

Regarding claim 2, Sato and Shirasaki teach the apparatus according to claim 1, wherein said data driving circuit comprises: a switch which switches to a state in which the reset voltage is applied to said plurality of current lines in the first part of the selection period (Sato, S_1, …, S_n in Fig. 1); and a current source driver which supplies the designating current having the current value corresponding to the image signal after the reset voltage is applied by the switch within the selection period (Sato, Data Driver 3 in Fig. 1, "*the gradation designating current is the sink current flowing to the data driver 3 from the signal lines Y1 to Yn via the current terminals* OT_1 *to* O_{Tn}*, and is equal to the current value of the current flowing through the organic EL elements* $E_{1,1}$ *to Em,n in order to emit the light at the luminance gradation in accordance with image data*.", p. 27:5-12. See also p. 39:9-15, p. 40:16-24, see also Fig. 8, *Id*).

Regarding claim 3, Sato and Shirasaki teach the apparatus according to claim 1, further comprising a plurality of light-emitting elements which are arranged at intersections of said plurality of selection scan lines and said plurality of current lines (Sato, $E_{i,j}$ shown in Fig. 1), emit light at luminance corresponding to a current value of a driving current (Sato, p. 1:10-11, "*the emission luminance is set in accordance with the current value of a gradation signal outputted from the data driver 3*." p.20:15-18, p. 27), and each have two electrodes one of which is connected to a corresponding one of said plurality of pixel circuits (Sato, Fig. 1; Shirasaki, Fig. 1).

Regarding claim 4, Sato and Shirasaki teach the apparatus according to claim 3, wherein the reset voltage applied by the data driving circuit is set equal to or lower than a voltage of the other electrode of the light-emitting element(Shirasaki discloses that the reset voltage applied by the data driving circuit (Vreset) is ground, which is equal to the voltage of the "other electrode of the light-emitting element," i.e., the cathode, which is also grounded. For example, Shirasaki discloses that Vreset is ground: "*At the beginning of the select period, the data line is grounded by Vreset to discharge the data line and the OLEO anode*." p. 1 or p. 1665, Shirasaki.)

Regarding claim 5, Sato and Shirasaki teach the apparatus according to claim 1, further comprising: a plurality of voltage supply lines (Sato, Z_1-Z_m, Fig. 1; Shirasaki, V_{source} lines); and a voltage supply driver (Sato, power supply scanning driver 6, Fig. 1; Shirasaki, driver that supplies V_{source}) which sequentially selects said plurality of voltage supply lines in synchronism with the sequential selection of said plurality of selection scan lines by the selection scan driver (Sato, Fig. 8, V_{ON} and V_{DD} are synchronized; Shirasaki, Fig. 2, see the synchronization between V_{select} and $V_{sournce}$).

Regarding claim 6, Sato and Shirasaki teach the apparatus according to claim 5, wherein each of said pixel circuits comprises:

a first transistor having a gate connected to the selection scan line (Sato, 21 is connected to X_1; Shirasaki, T_2 is connected to the bus line V_{select}, Fig. 1), and a drain and source one of which is connected to the current line (Sato, source terminal of 21 is connected to Y_1; Shirasaki, source terminal of T_2 is connected to the bus line I_{data}, Fig. 1);

a second transistor having a gate connected to the selection scan line, and a drain and source one of which is connected to the voltage supply line (Sato. 22 in Fig. 1; Shirasaki, T_1 in Fig. 1);

a driving transistor having a gate connected to the other of the drain and source of the second transistor, and a drain and source one of which is connected to the voltage supply line, and the other of which is connected to the other of the drain and source of the first transistor(Sato, 23 in Fig. 1; Shirasaki, T_3 in Fig. 1); and

a capacitor which stores a gate-to-one of source and drain voltage of the driving transistor by holding the voltage (Sato, 24 in Fig. 1; Shirasaki, Cs in Fig. 1, p. 1 or p. 1665).

Claim 10 is a broader version of claim 3. Therefore, Sato and Shirasaki teach claim 10 as explained above for claim 3.

Regarding claim 11, Sato discloses a display panel driving method comprising:

sequentially selecting a plurality of selection scan lines of a display panel (Fig. 8, 5 in Fig. 1. Last paragraph of p. 24, see also pp. 37, 39 and the description associated with the

selection scanning driver 5 in Fig. 1) comprising a plurality of pixel circuits connected to the plurality of selection scan lines and a plurality of current lines (Fig. 1, pixel circuits $P_{i,j}$), and a plurality of light-emitting elements which are arranged at intersections of the plurality of selection scan lines and the plurality of current lines (Fig. 1, Ei,j shown in Fig. 1), wherein each of the light-emitting elements emits light at luminance corresponding to a current value of a current flowing the current line (p. 1:10-11, "*the emission luminance is set in accordance with the current value of a gradation signal outputted from the data driver 3*." p.20:15-18, p. 27);

applying a reset voltage to the plurality of current lines [in an initial part of a period] in which each of the plurality of selection scan lines is selected (V_R is the reset voltage, pp. 31-32, "*The switch circuits S1 to Sn are connected to a reset voltage input terminal 141, and the reset voltage VR is applied to the switch circuits S1 to Sn via this terminal*." See Also Fig. 8);

after applying the reset voltage, supplying designating currents having current value corresponding to an image signal to the plurality of current lines ("*the gradation designating current is the sink current flowing to the data driver 3 from the signal lines Y1 to Yn via the current terminals OT_1 to O_{Tn}, and is equal to the current value of the current flowing through the organic EL elements $E_{1,1}$ to Em,n in order to emit the light at the luminance gradation in accordance with image data*.", p. 27:5-12. See also p. 39:9-15, p. 40:16-24, see also Fig. 8).

However Sato does not expressly discloses "applying a reset voltage to the plurality of current lines in an initial part of a period in which each of the plurality of selection scan lines is selected" and "storing, in the plurality of pixel circuits, the current value of the designating currents flowing through the plurality of current lines; and after supplying the designating currents, allowing the plurality of pixel circuits to supply, to the plurality of light-emitting

elements, driving currents having current value corresponding to the stored current value of the designating currents."

In the same field of display devices, data driving circuit and display panel driving method, Shirasaki discloses a "*full color polymer OLED display driven by a-Si:H TFT utilizing a new current-programmed method*" (Shirasaki, title). Shirasaki discloses an OLED display for TV monitor application and "*the panel for this application is required to be driven by an active-matrix (AM) method and to have a larger panel-size*" (INTRODUCTION, *Id*).

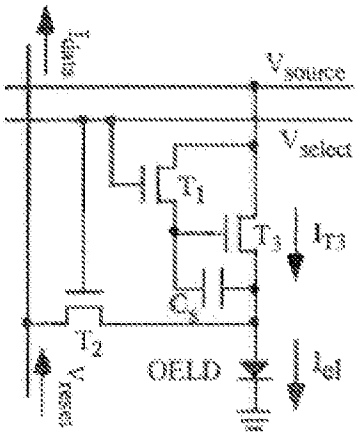

Fig.1 3 Tr pixel driver circuit

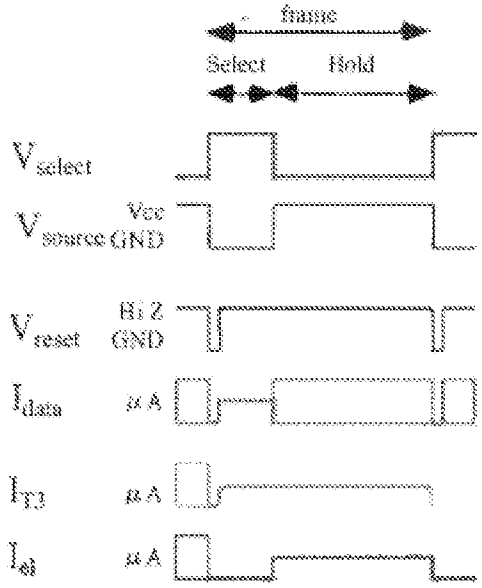

Fig.2 Timing diagram

-Figs. 1 and 2 of Shirasaki.

Shirasaki discloses:

> Figures 1 and 2 show a pixel driver circuit and a timing diagram of the signals, respectively. At the beginning of the select periods, the data line is grounded by V_{reset} to discharge the data line and the OLED anode. Then I_{data} is set to the pixel circuit with a sink mode. To prevent the current flow through the OLED, V_{source} is also grounded and the OLED is biased reversely. Therefore I_{data} corresponds to I_{T3} and C_S stores the voltage to keep the I_{T3}. During the hold period, V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on C_S.

-Pixel Circuit and A set of Timing, p.1 or p. 1665, *Id*.

Table 1 of Shirasaki discloses that its display includes a matrix comprising 160 columns and 128 rows of pixels and its "3-TFT and 3-busline pixel circuits" provided for each of the 160X128 pixels. For example, for each pixel of the display panel, there is one pixel driver circuit shown in Fig. 1. Because Shirasaki discloses a 2.1inch OLED display (Fig. 5) with plurality of pixels, Shirasaki discloses a plurality of pixel driver circuits. Further, the V_{select} lines are the selection scan lines, and for each row of pixels, there will be one V_{select} line (Fig. 1, *Id*). The I_{data} lines are the current lines and for each column of pixels, there is one I_{data} line (Fig. 1, *Id*) and the I_{data} lines correspond to I_{T3} and Cs stores the voltage to keep the I_{T3}. Shirasaki discloses "a selection scan driver" for V_{select} that provides the signals disclosed in Fig. 2.

Shirasaki discloses that a data driving circuit applies a reset voltage to said plurality of current lines in a first part of the selection period (Fig. 2, Vreset is applied in the first part of the selection period) and that in the "selection period", each of the "pixel circuits loads the designating current (I_{data}) which flows through said plurality of current line" and each pixel circuit stores a level of a voltage converted in accordance with the current value of the designating current (Cs stores the voltage to keep the I_{T3}).

Shirasaki discloses at the end of select period, I_{data} no longer flows to the pixel (Fig. 2). Shirasaki further explains that during the "hold" period (Fig. 2), "V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on Cs" (p. 1 or p. 1665, *Id*).

Table 1 Specifications

Items	Specification	
Size (Diagonal)	5.2 (2.1)	cm (inch)
Dot format	160(H)×RGB×128(V)	dot
Dot pitch	0.252(H)×0.252(V)	mm
Flame frequency	30	Hz
Color arrangement	RGB-stripe	
Input signal	RGB each 6-bit	
CIE Color Coordinate	R (0.69, 0.31) G (0.40, 0.58) B (0.15, 0.15)	
Contrast Ratio	> 100 : 1	

-Table. 1 of Shirasaki.

As explained above and shown in Figs. 1-2 and above cited paragraph of Shirasaki, Shirasaki discloses or suggests

> storing, in the plurality of pixel circuits, the current value of the designating currents flowing through the plurality of current lines; and after supplying the designating currents, allowing the plurality of pixel circuits to supply, to the plurality of light-emitting elements, driving currents having current value corresponding to the stored current value of the designating currents.

TSM-motivation

Shirasaki discloses:

> There are two ways to compensate the TFT threshold voltage variation, current-program [2] and voltage-program [3]. Both of them needed more than four TFTs; and four bus-lines for each pixel. in general, which is too complicated in driving scheme and too busy in pixel aria to achieve the high reliability and large aperture ratio. Simpler circuit design and driving scheme are expected in a-Si TFT driving AM--OLED, In SID'03 three TFT voltage-program pixel circuit was presented using in 20 inch a-Si TFT AM-OLED [4]. This driving technology makes possible to drive large-sized AM-OLED utilizing a-Si TFT.

-Introduction, Shirasaki.

It is desirable to be able to drive a large-size AM-OLED and have a simpler driving scheme to achieve high reliability and large aperture ratio. Therefore it would have been obvious to one of ordinary skills in the art, at the time of invention of the `042 Patent to use Shirasaki's algorithm of data driving in data driving circuits and the algorithm of the pixel circuits in the display device of Sato so that large-size AM-OLED can be driven with high reliability and large aperture ratio.

KSR-motivation

The combination of Sato with Shirasaki is supported by KSR rationale - (C) Use of known technique to improve similar devices (methods, or products) in the same way because: (1) as discussed above, Sato teaches a method performing in a base device that is the same as the invention, except for improvements, such as, the features noted as missing above; (2) Sato and Shirasaki are similar methods performed by similar devices; and (3) the references show that a POSITA at the time of the invention had the skill set and could apply Shirasaki's method of operating the data driving circuits and pixel circuits to improve the base device of Sato in the same way with predictable results or (B) Simple substitution of one known element for another to obtain predictable results because substituting the algorithm of the data driving circuits and the algorithm of the pixel circuits of Sato by that of Shirasaki will obtain predictable results.

B. Claims 1-6 and 10-11 are rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Shirasaki in view of Sato.

Summary of Rejection. Shirasaki discloses the selection scan lines, the current lines. the pixel circuits and the algorithm performed by the pixel circuits. However, Shirasaki does not expressly disclose the selection scan driver, the data driving circuits and their algorithms. The

secondary reference of Sato discloses the selection scan driver and the data driving circuits and their algorithms.

Regarding claim 1, Shirasaki teaches a display device comprising:

a plurality of selection scan lines (V_{select} bus lines, Fig. 1 and 5, Table 1, there must be a plurality of V_{select} because there are 128 rows of pixels and there is one for each row of pixels. See also Fig. 2);

a plurality of current lines (I_{data} lines is the current used to program the pixel, Fig. 1 and 5, Table 1, there must be a plurality of I_{data} lines because there are 160 column of pixels and there is one for each column of pixels. See also Fig. 2);

a selection scan driver which sequentially selects said plurality of selection scan lines in each selection period ("*the panel for this application is required to be driven by an active-matrix method*," p. 1 or p. 1665, see Fig. 2 which shows in a selection period, a V_{select} is turned on to drive the display. Each row of pixels requires one selection scan line V_{select}.);

a data driving circuit which applies a reset voltage to said plurality of current lines in a first part of the selection period (Fig. 1, each column of pixels requires a I_{data} and V_{reset} line, "*at the beginning of the select period, the data line is grounded by V_{reset} to discharge the data line and the OLED anode*." p.1 or p. 1665, Fig.2 shows the reset voltage applied during a first part of the selection period), and supplies a designating current having a current value corresponding to an image signal to said plurality of current lines in a second part of the selection period after applying the reset voltage in the selection period (Fig. 2 shows after Vreset is set to ground, current I_{data} is supplied. See also p. 1 or p. 1665. Also inherent because "*active matrix driving*

method" at p. 1 or p. 1665 must supplies a designating current having a current value corresponding to an image signal. Fig. 1); and

a plurality of pixel circuits which are connected to said plurality of selection scan lines and said plurality of current lines (Fig. 1, each pixel circuit is connected to a selection scan line (V_{select}) and a current line (I_{data}/V_{reset}). Table 1, because a display panel with 160X128 pixels is disclosed, there are a plurality of pixel circuits. The pixel circuits are "*3-TFT and 3 busline pixel circuits.*" Abstract, p. 1 or p. 1665), and supply a driving current having a current value corresponding to the current value of the designating current which flows through said plurality of current lines ("*Then Idata is set to the pixel circuit with a sink mode. To prevent the current flow through the OLEO, V_{source} is also grounded and the OLED is biased reversely.*" p. 1 or p. 1665. See also Fig. 2);

wherein in the selection period, each of said plurality of pixel circuits loads the designating current which flows through said plurality of current lines ("*Then Idata is set to the pixel circuit with a sink mode. To prevent the current flow through the OLEO, V_{source} is also grounded and the OLED is biased reversely.*" p. 1 or p. 1665, see also Fig. 2), and stores a level of a voltage converted in accordance with the current value of the designating current ("*Therefore I_{data} corresponds to I_{T3} and Cs stores the voltage to keep the I_{T3}*", p. 1 or p. 1665, the storage capacitor Cs stores a voltage that corresponds to the designating current), and after the selection period, each of said plurality of pixel circuits shuts off the designating current which flows through said plurality of current lines, and supplies a driving current corresponding to the level of the voltage converted in accordance with the designating current ("*during the hold period, V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on Cs*", p. 1 or p. 1665. See also Fig. 2).

Shirasaki discloses a display panel with 160x128 pixels implemented by the 3-TFT and 3-buslines pixel circuits in Fig. 1 (see also Table 1, p. 1 or p. 1665). Shirasaki also uses "an active matrix driving" method (p. 1 or p. 1665). To the extent that Shirasaki does not inherently disclose the structure of the selection scan driver and the data driving circuits as disclosed by the `042 Patent for performing the functions as recited in claim 1 by these two components respectively, Sato discloses or suggests the structure of the selection scan driver and the data driving circuits as explained below.

In the same field of display devices and display driving method (p. 1), Sato discloses a display panel circuits shown in Fig. 1 with a selection scan driver comprising shifter registers ("*the selection scanning driver 5 is formed of a so-called shifter register*." p. 24) and the data driving circuits comprising a data driver (3 in Fig. 1) and a current/voltage changeover portion 7.

A POSITA would have recognized that Sato's use of selection scan driver and a data driving circuit would readily apply to Shirasaki's device, which also discloses a pixel circuit connected to a signal line that alternates between V_{reset} and I_{data}.

A POSITA would have understood that a straightforward way to implement Shirasaki's selection scan driver and the data driving circuits of providing the reset voltage V_R followed by the designating current I_{data} on the same signal line would be through Sato's disclosed selection scan driver and data driving circuit, which also provides both a reset voltage and a designating current to the same signal line. This would have been nothing more than the use of a known technique in a known device, and one of only a few well-known and understood possibilities for implementing the provision of multiple signals on the same signal line with the timings disclosed by Shirasaki.

A POSITA would have further recognized that the results would be predictable and would have had a reasonable expectation of success, because as explained above Sato discloses that its data driving circuit provides both a reset voltage and a designating current to a current line connected to the same pixel circuit disclosed in Shirasaki. See also MPEP 2143.

Therefore it would be obvious to a POSITA, at the time of invention of the `042 Patent, to implements the circuits of Shirasaki as that in Sato to have a complete display panel.

Regarding claim 2, Shirasaki in view of Sato teach the apparatus according to claim 1, wherein said data driving circuit comprises: a switch which switches to a state in which the reset voltage is applied to said plurality of current lines in the first part of the selection period (Sato, S_1, …, S_n in Fig. 1); and a current source driver which supplies the designating current having the current value corresponding to the image signal after the reset voltage is applied by the switch within the selection period (Sato, Data Driver 3 in Fig. 1, "*the gradation designating current is the sink current flowing to the data driver 3 from the signal lines Y1 to Yn via the current terminals* OT_1 *to* O_{Tn}*, and is equal to the current value of the current flowing through the organic EL elements* $E_{1,1}$ *to Em,n in order to emit the light at the luminance gradation in accordance with image data*.", p. 27:5-12. See also p. 39:9-15, p. 40:16-24, see also Fig. 8, *Id*).

Regarding claim 3, Shirasaki in view of Sato teach the apparatus according to claim 1, further comprising a plurality of light-emitting elements which are arranged at intersections of said plurality of selection scan lines and said plurality of current lines (Sato, $E_{i,j}$ shown in Fig. 1), emit light at luminance corresponding to a current value of a driving current (Sato, p. 1:10-11, "*the emission luminance is set in accordance with the current value of a gradation signal*

outputted from the data driver 3." p.20:15-18, p. 27:), and each have two electrodes one of which is connected to a corresponding one of said plurality of pixel circuits (Sato, Fig. 1; Shirasaki, Fig. 1).

Regarding claim 4, Shirasaki in view of Sato teach the apparatus according to claim 3, wherein the reset voltage applied by the data driving circuit is set equal to or lower than a voltage of the other electrode of the light-emitting element(Shirasaki discloses that the reset voltage applied by the data driving circuit (Vreset) is ground, which is equal to the voltage of the "other electrode of the light-emitting element" (i.e., the cathode, which is also grounded). For example, Shirasaki discloses that Vreset is ground: "*At the beginning of the select period, the data line is grounded by Vreset to discharge the data line and the OLEO anode*." P. 1 or p. 1665, Shirasaki.)

Regarding claim 5, Shirasaki in view of Sato teach the apparatus according to claim 1, further comprising: a plurality of voltage supply lines (Sato, Z_1-Z_m, Fig. 1; Shirasaki, V_{source} lines); and a voltage supply driver (Sato, power supply scanning driver 6, Fig. 1; Shirasaki, the driver that supplies V_{source}) which sequentially selects said plurality of voltage supply lines in synchronism with the sequential selection of said plurality of selection scan lines by the selection scan driver (Sato, Fig. 8, V_{ON} and V_{DD} are synchronized; Shirasaki, Fig. 2, see the synchronization between V_{select} and $V_{sournce}$).

Regarding claim 6, Shirasaki in view of Sato teach the apparatus according to claim 5, wherein each of said pixel circuits comprises:

a first transistor having a gate connected to the selection scan line (Sato, 21 is connected to X_1; Shirasaki, T_2 is connected to the bus line V_{select}, Fig. 1), and a drain and source one of which is connected to the current line (Sato, Fig. 1, source terminal of 21 is connected to Y_1; Shirasaki, source terminal of T_2 is connected to the bus line I_{data}, Fig. 1);

a second transistor having a gate connected to the selection scan line, and a drain and source one of which is connected to the voltage supply line (Sato, Fig. 1, 22 in Fig. 1; Shirasaki, Fig. 1, T_1 in Fig. 1);

a driving transistor having a gate connected to the other of the drain and source of the second transistor, and a drain and source one of which is connected to the voltage supply line, and the other of which is connected to the other of the drain and source of the first transistor(Sato, Fig. 1, 23 in Fig. 1; Shirasaki, Fig. 1, T_3 in Fig. 1); and

a capacitor which stores a gate-to-one of source and drain voltage of the driving transistor by holding the voltage (Sato, Fig. 1, 24 in Fig. 1; Shirasaki, Fig. 1, Cs in Fig. 1, p. 1 or p. 1665).

Claim 10 is a broader version of claim 3. Therefore, Shirasaki in view of Sato teach claim 10 as explained above for claim 3.

Regarding claim 11, Shirasaki teaches a display panel driving method comprising:

sequentially selecting a plurality of selection scan lines of a display panel ("*the panel for this application is required to be driven by an active-matrix method*," p. 1 or p. 1665, see Fig. 2 which shows in a selection period, a V_{select} is turned on to drive the display. Each row of pixels requires one selection scan line V_{select}.) comprising a plurality of pixel circuits (Fig. 1, each pixel circuit is connected to a selection scan line (V_{select}) and a current line (I_{data}/V_{reset}). Table 1,

because a display panel with 160X128 pixels is disclosed, there are a plurality of pixel circuits. The pixel circuits are "*3-TFT and 3 busline pixel circuits.*" Abstract, p. 1 or p. 1665) connected to the plurality of selection scan lines (V_{select} bus lines, Fig. 1 and 5, Table 1, there must be a plurality of V_{select} because there are 128 rows of pixels and there is one for each row of pixels. See also Fig. 2) and a plurality of current lines (I_{data} lines is the current used to program the pixel, Fig. 1 and 5, Table 1, there must be a plurality of I_{data} lines because there are 160 column of pixels and there is one for each column of pixels. See also Fig. 2), and a plurality of light-emitting elements (OLED or OELD in Fig. 1, inherent because each pixel must have one) which are arranged at intersections of the plurality of selection scan lines and the plurality of current lines (Fig. 1), wherein each of the light-emitting elements emits light at luminance corresponding to a current value of a current flowing the current line (inherent from the property of an OLED or OELD);

applying a reset voltage to the plurality of current lines in an initial part of a period in which each of the plurality of selection scan lines is selected (Fig. 1, each column of pixels requires a I_{data} and V_{reset} line, "*at the beginning of the select period, the data line is grounded by V_{reset} to discharge the data line and the OLED anode.*" p.1 or p. 1665, Fig.2 shows the reset voltage applied during a first part of the selection period);

after applying the reset voltage, supplying designating currents having current value corresponding to an image signal to the plurality of current lines (Fig. 2 shows after Vreset is set to ground, current I_{data} is supplied. See also p. 1 or p. 1665. Also inherent because "*active matrix driving method*" at p. 1 or p. 1665 must supplies a designating current having a current value corresponding to an image signal. Fig. 1), and

storing, in the plurality of pixel circuits, the current value of the designating currents flowing through the plurality of current lines ("*Therefore I_{data} corresponds to I_{T3} and Cs stores the voltage to keep the I_{T3}*", p. 1 or p. 1665, the storage capacitor Cs stores a voltage that corresponds to the designating current); and

after supplying the designating currents, allowing the plurality of pixel circuits to supply, to the plurality of light-emitting elements, driving currents having current value corresponding to the stored current value of the designating currents ("*during the hold period, V_{source} is set to be V_{cc} and I_{T3} keeps flowing according to the voltage on Cs*", p. 1 or p. 1665. See also Fig. 2)..

To the extent that Shirasaki does not inherently discloses a plurality of selection scan lines, a plurality of current lines, a plurality of pixel circuits and wherein each of the light-emitting elements emits light at luminance corresponding to a current value of a current flowing the current line, Sato discloses them.

Shirasaki discloses a display panel with 160x128 pixels implemented by the 3-TFT and 3-buslines pixel circuits in Fig. 1 (see also Table 1, p. 1 or p. 1665). Shirasaki also uses "an active matrix driving" method (p. 1 or p. 1665). To the extent that Shirasaki does not inherently disclose a plurality of selection scan lines, a plurality of current lines, a plurality of pixel circuits and wherein each of the light-emitting elements emits light at luminance corresponding to a current value of a current flowing the current line, Sato discloses them.

In the same field of display devices and display driving method (p. 1), Sato discloses a display panel circuits shown in Fig. 1 with a selection scan driver comprising shifter registers ("*the selection scanning driver 5 is formed of a so-called shifter register*." p. 24) and the data driving circuits comprising a data driver (3 in Fig. 1) and a current/voltage changeover portion 7. Sato further discloses each of the light-emitting elements emits light at luminance corresponding

to a current value of a driving current (Sato, p. 1:10-11, "the emission luminance is set in accordance with the current value of a gradation signal outputted from the data driver 3." p.20:15-18, p. 27).

A POSITA would have recognized that Sato's plurality of selection scan lines and current lines and a plurality of pixel circuits and the use of OLED would readily apply to Shirasaki's device and method to extend the pixel circuits to accommodate a display panel comprising 160X128 pixels.

A POSITA would have understood that a straightforward way to implement Shirasaki's plurality of selection scan lines and current lines and a plurality of pixel circuits would be through Sato's disclosed scan lines and current lines and pixel circuits, which also provides the method steps as recited in claim 11. This would have been nothing more than the use of a known technique in a known device, and one of only a few well-known and understood possibilities for implementing the provision of data driving by active matrix programming by Shirasaki.

A POSITA would have further recognized that the results would be predictable and would have had a reasonable expectation of success, because as explained above Sato discloses that the plurality of pixel circuits connected by selection scan lines and current lines provide the same functionality disclosed in Shirasaki. See also MPEP 2143.

Therefore it would be obvious to a POSITA, at the time of invention of the `042 Patent, to implements the circuits and method of Shirasaki as that in Sato to have a complete display panel.

C. Claim 11 is rejected under pre-AIA 35 U.S.C. § 103(a) as being unpatentable over Miyazawa.

Summary of Rejection. This ground of rejection is based on two embodiments of Miyazawa and all the claim limitations are disclosed by the two embodiments of Miyazawa.

Regarding claim 11, Miyazawa discloses a display panel driving method comprising:

sequentially selecting a plurality of selection scan lines of a display panel comprising a plurality of pixel circuits connected to the plurality of selection scan lines and a plurality of current lines (Fig. 2, "[0038] *The gate driver 300 selectively drives one of the plurality of gate lines Yn and selects one row of pixel circuits. The data line driver 400 has a plurality of single-line drivers 400 that individually drive the data lines Xm. These single-line drivers 410 supply data signals to the pixel circuits 210 over the data lines Xm. When the internal state (to be described below) of each pixel circuit 210 is set via these data signals, the value of the current flowing to each organic EL element 220 is controlled based on such setting, and as a result, the tone of the light emission from each organic EL element is controlled*." See also ¶ ¶ [0053] and [0086]-[0088]), and a plurality of light-emitting elements which are arranged at intersections of the plurality of selection scan lines and the plurality of current lines, wherein each of the light-emitting elements emits light at luminance corresponding to a current value of a current flowing the current line (Fig. 2, ¶ [0037] "*…each pixel circuit 210 has an organic EL element 220*." ¶ [0059], "*Because the voltage corresponding to the programming current value Im is stored in advance in the holding capacitor 230, a current that is essentially equivalent to the programming current value Im flows to the fourth transistor 214. Therefore, a current that is essentially equivalent to the programming current value Im also flows to the organic EL element 220, which emits light having a tone corresponding to this current value Im.*");

applying a reset voltage to the plurality of current lines in an initial part of a period in which each of the plurality of selection scan lines is selected (Figs. 13(a)-13(e), ¶ [0087], "*During the first half of the programming period Tpr, voltage programming is executed through the supply of a voltage signal Vout (see FIG. 13(c)) from the voltage generating circuit 411d to the data line Xm. When this is done, the data line Xm is charged or discharged and the holding capacitor 230 is charged or discharged accordingly*." See also Fig. 13 which shows the timing chart and ¶ ¶ [0043]-[0044] and [0086] and [0088]);

after applying the reset voltage, supplying designating currents having current value corresponding to an image signal to the plurality of current lines (¶ [0087], "*During the second half of the programming period Tpr, the holding capacitor 230 is accurately programmed through the supply of a current signal Iout (FIG. 13(d)) from the current generating circuit 412d*." see also Fig. 13 and ¶ ¶ [0056]-[0057] and [0088]), and

storing, in the plurality of pixel circuits, the current value of the designating currents flowing through the plurality of current lines (¶ [0087], "*During the second half of the programming period Tpr, the holding capacitor 230 is accurately programmed through the supply of a current signal Iout (FIG. 13(d)) from the current generating circuit 412d*." see also Fig. 13 and ¶ ¶ [0057]-[0059] and [0088]); and

after supplying the designating currents, allowing the plurality of pixel circuits to supply, to the plurality of light-emitting elements, driving currents having current value corresponding to the stored current value of the designating currents (Fig. 13 and ¶ ¶ [005]-[0059] and [0042], "*The holding capacitor 230 maintains an electric charge commensurate with the current value of the current signal Iout supplied thereto via the second sub-data line U2, and thereby adjusts the tone of the light emission from the organic EL element 220. In this example, the first through*

third transistors 211-213 are n-channel FETs, while the fourth transistor 214 is a p-channel FET. Because the organic EL element 220 is a current infusion (current-driven) type light-emitting element similar to a photodiode, it is expressed in the figure using a diode symbol.").

The cited disclosures above are from Embodiment 1 and Embodiment 5 of Miyazawa.

Miyazawa discloses:

> [0086] FIG. 12 is a circuit diagram showing the internal constructions of a pixel circuit 210d and a single-line driver 410d of a fifth embodiment. This pixel circuit 210d is identical to the circuit shown in FIG. 4. In other words, the fifth embodiment does not have the two switching transistors 251 and 252 that were present in the first embodiment (see FIG. 3). Furthermore, the sub-gate line V1 used for the transistors 251 and 252 is also omitted. The single-line driver 410d and its internal circuits 411d and 412d are identical to the equivalent circuits in the first embodiment shown in FIG. 3. However, the fifth embodiment differs from the first embodiment in that the voltage generating circuit 411d and the current generating circuit 412d are commonly connected to the pixel circuit 210d via a single data signal line Xm.
>
> [0088] … In the fifth embodiment in particular, current programming is executed after the completion of voltage programming using the same single data line Xm. During voltage programming, a kind of pre-charge is executed with respect to both the data line Xm and the holding capacitor 230, whereupon current programming is executed. Therefore, the light emission tone can be set more accurately and quickly than is possible using the pixel circuit of the conventional art.

-¶¶[0086] and [0088] of Miyazawa.

As disclosed by Miyazawa above, Embodiment 5 is merely modifying some structure of the pixel circuits and programming of the driving circuits and is based on Embodiment 1 with improvements.

Therefore it would be obvious to POSTIA, at the time of invention of the `042 Patent, to combine the teaching of Embodiment 5 of Miyazawa with the Embodiment 1 of Miyazawa or modify the Embodiment 1 of Miyazawa to arrive at Embodiment 5 of Miyazawa so that the light

emission tone can be set more accurately and quickly than is possible using the pixel circuit of the conventional art.

The combination of Embodiment 1 and Embodiment 5 of Miyazawa is also supported by KSR Rationale (C) Use of known technique to improve similar devices (methods, or products) in the same way because using the techniques in Embodiment 5 of Miyazawa will improve Embodiment 1 of Miyazawa because the light emission tone can be set more accurately and quickly.

VIII. EX PARTE REEXAMINATION REMINDER

A. Specific Explanation of Support Must be Provided

37 CFR 1.530 (e) states:

> (e) Status of claims and support for claim changes. Whenever there is an amendment to the claims pursuant to paragraph (d) of this section, there must also be supplied, on pages separate from the pages containing the changes, the status (i.e., pending or canceled), as of the date of the amendment, of all patent claims and of all added claims, and an explanation of the support in the disclosure of the patent for the changes to the claims made by the amendment paper.

In other words, explanation of support of changes made to claims including amended claims and new claims must be provided and specific.

B. Amended Claims or New Claims Cannot be Broadened.

37 CFR 1.552 (b) states:

> (b) Claims in an ex parte reexamination proceeding will not be permitted to enlarge the scope of the claims of the patent.

MPEP 2258 states:

> A reexamination proceeding ordered under 35 U.S.C. 304 provides a complete reexamination of the patent claims on the basis of prior art patents and printed

publications. Double patenting issues may also be considered during reexamination. See subsection I.D. below. Issues relating to 35 U.S.C. 112 are addressed only with respect to new claims or amendatory subject matter in the specification, claims or drawings. Any new or amended claims are examined to ensure that the scope of the original patent claims is not enlarged, i.e., broadened. See 35 U.S.C. 305.

Therefore the Patent Owner is reminded that any new or amended claims cannot be broadened.

IX. NOTICE RE PATENT OWNER'S CORRESPONDENCE ADDRESS

37 C.F.R. § 1.33(c) states:

(c) All notices, official letters, and other communications for the patent owner or owners in a reexamination or supplemental examination proceeding will be directed to the correspondence address in the patent file.

The correspondence address for any pending reexamination proceeding not having the same correspondence address as that of the patent is, by way of this revision to 37 C.F.R. § 1.33(c), automatically changed to that of the patent file as of the effective date.

In the event the patent owner's correspondence address listed in the papers (record) for the present proceeding is different from the correspondence address of the patent, it is strongly encouraged that the patent owner affirmatively file a Notification of Change of Correspondence Address in the reexamination proceeding and/or the patent (depending on which address patent owner desires), to conform the address of the proceeding with that of the patent and to clarify the record as to which address should be used for correspondence.

Telephone Numbers for reexamination inquiries:

Reexamination (571) 272-7703

X. CONCLUSION

Extensions of time under 37 C.F.R. § 1.136(a) will not be permitted in these proceedings because the provisions of 37 C.F.R. § 1.136 apply only to "an applicant" and not to parties in a reexamination proceeding. Additionally, 35 U.S.C. 305 requires that ex parte reexamination proceedings "will be conducted with special dispatch" (37 C.F.R. § 1.550(a)). Extensions of time in ex parte reexamination proceedings are provided for in 37 C.F.R. § 1.550(c).

Patent owner is reminded of the continuing responsibility under 37 C.F.R. § 1.565(a), to apprise the Office of any litigation activity, or other prior or concurrent proceeding, involving the 538 patent throughout the course of this reexamination proceeding. See MPEP §§ 2207, 2282 and 2286. The third party requester is similarly apprised of the ability to disclose such proceedings.

Registered users of EFS-Web may alternatively submit correspondence via the electronic filing system at https://efs.uspto.gov/efile/myportal/efs-registered

Signed:

/YUZHEN GE/
Primary Examiner, Art Unit 3992

Conferees:

/NICK CORSARO/
Primary Examiner, Art Unit 3992

/ANDREW J. FISCHER/
Supervisory Patent Reexamination Specialist, Art Unit 3992